Some physical results of single electron transitor

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ABSTRACT

Single electron transistor (SET) is a key element in current research area of nanoelectronics and nanotechnology which can offer nano-feature size, low power consumption and high operating speed. SET is a new nanoscale switching device. It can control the motion of the single electron. The goal of this paper is to discuss about some physical properties of the SET and focuses on simulation of basic quantum device characteristics such as tunneling effect, Coulomb blockage, Quantum dot, Coulomb staircase, and Coulomb oscillation. The current-voltage characteristics of SET are explored for illustration. Two types of metallic and semiconducting SETs have been simulated.

***Key words**: single electron transistor, current-voltage characteristics, Coulomb blockage, Coulomb staircase, Coulomb oscillation*

INTRODUCTION

Rapid progress in microelectronics has pushed the MOSFET (dimension toward the physical limit (10 nm). In the future it is probable that the nano-MOSFETs could be replaced by new fundamental devices such as single electron transistor (SET). SETs have attracted much attention for IC applications because of their nano-feature size, ultra-low power dissipation, high frequency, new functionalities, and CMOS compatible fabrication process [1].

After their discovery in the 1986 [2, 3], there has been extensive research on the fabrication, design and modeling of SETs [4]. SETs with a variety of structures were proposed and fabricated by using different methods [5-7]. SETs have been fabricated to operate at room temperature [8-10]. Molecular quantum dot [11] can display SET's behavior. 1D structures, such as carbon nanotubes and nanowires, can act as SETs [7]. Recent advances in grapheme [12] show promise for SETs.

Research on SET modeling and simulation has been an active area. Monte Carlo simulation has been widely used to model SETs. SIMON [13] and MOSES [14] are the two most popular SET simulators. Uchida et al. proposed an analytical SET model and incorporated it into SPICE [15]. Inokawa et al. extended this model to a more general form to include asymmetric SETs [16]. Mahapatra et al. proposed a simulation framework for hybrid SET/CMOS circuit design and analysis [17]. In contrast, model used non-equilibrium Green's function method (NEGF) [18] commonly used in the nanoscale devices and are superior in terms of simplicity.

In this work, we introduce the physical properties of SET and simulate current-voltage characteristics in single electron transistor by non-equilibrium Green's function method using graphic user interface (GUI) of Matlab. Here, we use a model of one-level (metallic) and multiple-level (semiconducting) device for SET. We also summarize the theoretical approach based on NEGF, review the capabilities of the simulator, NEMO-VN2 [19], give examples of typical

simulations of SET's current-voltage characteristics, and compare simulated results with experimental ones.

PHYSICS, MODELING AND SIMULATION OF THE SINGLE ELECTRON TRANSISTOR

Basic physical properties of the single electron transistor

The operation of a single electron tunneling device is governed by the Coulomb charging effect. As shown in Fig. 1A, a single electron tunneling device consists of a nanometer-scale conductive (or semiconducting) island embedded in an insulating material. Electrons travel between the island, source (S) and drain (D) through thin insulating tunnel junctions. When an electron tunnels into the island, the overall electrostatic potential of the island increases by e/C_Σ, where e is the elementary charge and C_Σ is island capacitance. For large devices, this change in potential is negligible due to the high capacitance C_Σ. However, for nanometer-scale islands, C_Σ is much smaller (about aF).

Change to SET island potential results an energy gap at the Fermi energy, preventing further electron tunneling. This phenomenon is called Coulomb blockade. It prevents current from flowing between source and drain ($I_{ds} = 0$), i.e, the SET is turned off. The Coulomb blockade effect can be overcome by changing the voltage of a conductor gate capacitively coupled to the island, thereby turning tunneling on or off.

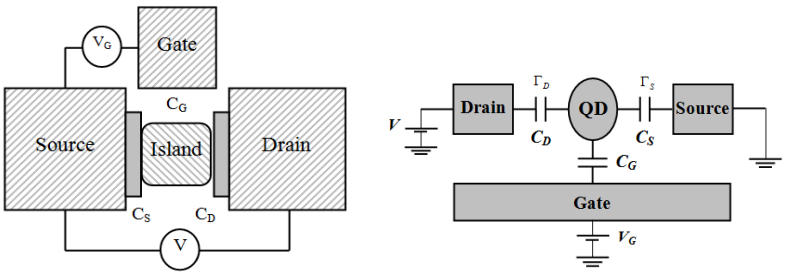
As shown in Fig. 1A SET typically has three terminals. The source and drain terminals serve as electron reservoirs. When the SET is turned on, electrons tunnel from one terminal, through the junction, to the conductive island. They then tunnel through the other junction to the other terminal. Each tunneling junction is modeled as resistor (R_S or R_D) and capacitor (C_S or C_D) in parallel.

A gate terminal (G), with coupling capacitance C_G, controls the transport of electrons. The Coulomb blockade effect is maximized when $V_{GS} = me/C_G$, where $m = \pm 1, \pm 2, \pm 3, \cdots$ because, at these voltages, the system is in minimum-energy state when an integer number of electrons are present on the island. The Coulomb blockade effect vanishes when $= \pm 1/2 , \pm 3/2, \cdots$, i.e., when m is a half-integer value because, at these voltages, the system is in a minimum-energy state when a half-integer number of electrons are present on the island. In this case, the single tunneling event does not move the system from a minimum energy state. Electrons can therefore tunnel, in single-file, through the island as determined by V_{DS}.

In order to observe the Coulomb blockade effect, the following constraints must be satisfied.

1) Since thermal fluctuations can suppress the Coulomb blockade effect, the electrostatic charging energy, e^2/C_Σ, must be much greater than k_BT, where k_B is Boltzmann's constant and T is the temperature. In order to ensure the reliability, $e^2/C_\Sigma \geq k_B T$ other more conservative, $e^2/C_\Sigma \geq 40k_B T$ constraint is enforced. These equations imply that the maximum allowed island capacitance is inversely proportioned to temperature. At room temperature, an island capacitance below 1 aF is required. Island capacitance is a function of island size. As shown in Table 1 room temperature operation requires an island size in the nanometer range, making fabrication challenging. At present, the smallest island capacitance of a fabricated device is around 0.15 aF [9].

2) To observe single-electron charging effects, electrons must be confined to the island, which requires that the junction resistance must be higher than the quantum resistance, i.e., R_S, $R_D > h/e^2$, $h/e^2 = 25.8$ kΩ, where h is Plank's constant. Therefore, SETs have high resistances and low driving current.



(A) (B)

Figure 1. (A) Structure of SET, (B) equivalent schematic diagram of SET: C_G - gate capacitance, C_S - source tunnel junction capacitance, C_D – drain tunnel junction capacitance, R_S – source tunnel junction resistance, R_D – drain tunnel junction resistance

Simulation method and results

From the point of view of fabrication methods, single electron transistors can be divided into two categories: SET with metallic island (namely metallic SET) and semiconducting island (namely semiconducting SET). SET's models can be also grouped in one level device and multi-level device.

We describe a SET's model for metallic SET using one-level device. We describe a SET's model for a multiple-level device (semiconducting SET) whose energy levels are described by a Hamiltonian matrix [H] and whose coupling to the source and the drain contacts is described by self-energy matrices $[\Sigma_1(E)]$ and $[\Sigma_2(E)]$respectively (Fig. 2).

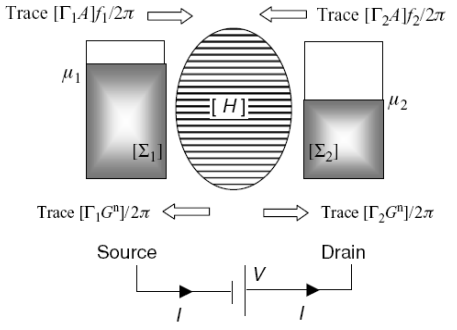


Fig. 2. Multi-level device whose energy levels are described by a Hamiltonian matrix [H] and whose coupling to the source and drain contacts is described by self-energy matrices$[\Sigma_1(E)]$ and $[\Sigma_2(E)]$ respectively

The flow of current is due to the difference in potentials between the source and the drain, each of which is in a state of local equilibrium, but maintained at different electro-chemical potentials $\mu_{1,2}$ and hence with two distinct Fermi functions:

$$f_1(E) = \frac{1}{exp\left[\left(E-\mu_1\right)/k_BT\right]+1} \quad (1)$$

$$f_2(E) = \frac{1}{exp\left[\left(E-\mu_2\right)/k_BT\right]+1} \quad (2)$$

by the applied bias V: $\mu_2 - \mu_1 = -qV$. Here, E-energy, k_B - Boltzmann constant, T- temperature. The density matrix is given by

$$\rho = \int_{-\infty}^{+\infty} \frac{dE}{2\pi} G^n(E) = \int_{-\infty}^{+\infty} \frac{dE}{2\pi} [A_1(E)f_1(E) + A_2(E)f_2(E)] \quad (3)$$

The current I_D flows in the external circuit is given by Landauer formula [18]:

$$I_D = (q/h) \int dET(E)\left(f_1(E) - f_2(E)\right) \quad (4)$$

The quantity T(E) appearing in the current equation (4) is called the transmission function, which tells us the rate at which electrons transmit from the source to the drain contacts by propagating through the device. Knowing the device Hamiltonian [H] and its coupling to the contacts described by the self-energy matrices $\Sigma_{1,2}$, we can calculate the current from (4). For coherent transport, one can calculate the

transmission from the Green's function method, using the relation:

$$T(E) = Trace[\Gamma_1 G \Gamma_2 G^+] + Trace[\Gamma_2 G \Gamma_1 G^+] \quad (5)$$

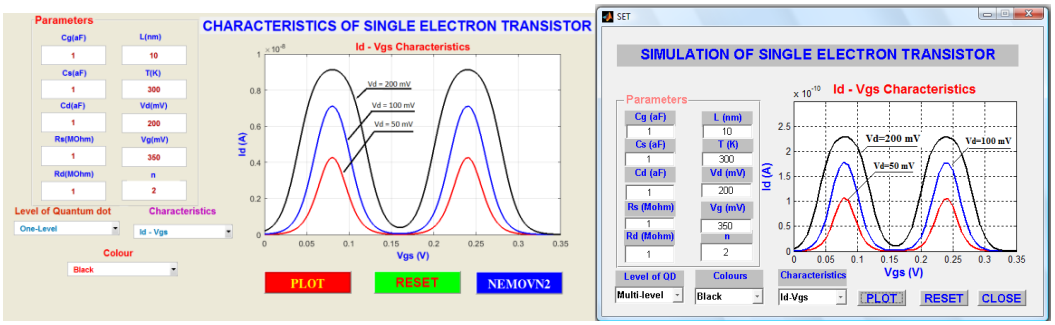
The appropriate NEGF equations are obtained:

$$G=[EI-H-\Sigma_1-\Sigma_2]^{-1}, \Gamma_{1,2}=i[\Sigma_{1,2}-\Sigma_{1,2}^+], A_1(E)=GI,$$
$$G^n=[A_1]f(E)+[A_2]f(E), \quad (6)$$
$$A=i[G-G^+]=[A_1]+[A_2]$$

Where H is effective mass Hamiltonian, I is an identity matrix of the same size, $\Gamma_{1,2}$ are the broadening functions, $A_{1,2}$ are partial spectral functions, A(E) are spectral function, G^n is correlation function. We use a discrete lattice with N points spaced by lattice spacing "a" to calculate the eigen-energies for electrons in the quantum dot.

By utilizing the simulator namely NEMO-VN2 [19], the I_D–V_G characteristics of SET having the given parameters are shown in Fig. 3.

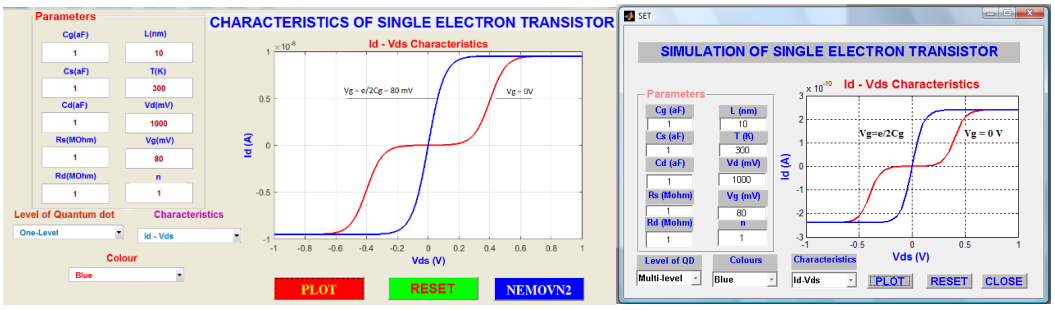
Fig. 3 demonstrates the typical Coulomb oscillation behavior in SET I_D-V_G characteristics. It shows that the SET Coulomb oscillation period (e/C_G, e is the electronic charge) is dictated by SET's gate capacitance. Values of gate voltage at the first and the second peaks are $e/2C_G$ (80 mV) and $3e/2C_G$ (240 mV) respectively. Here, it should be emphasized that the peak and the valley currents of Coulomb oscillations are perfectly represented by the model. The results calculated according to model ($e/2C_G$ for C_G = 1 aF) coincide well with the simulated ones. Current-voltage (I_D-V_G) characteristics showed the suppression of the Coulomb oscillation by broadening current peaks increased at high V_D (200 mV). It also reveals the fact that it is difficult to obtain the Coulomb oscillations in the device characteristics at high V_D greater than $3e/C_T$ (C_T is the total capacitance of SET), (160 mV). It should note that high drain voltage, V_D undermines SET's current-voltage characteristics. Characteristics of metallic and semiconducting SET are shown in Fig. 3A and 3B respectively.



(A) (B)

Fig. 3. Typical I_D-V_G characteristics (Coulomb oscillations) of SET simulated by the simulator NEMO-VN2 for various values of V_D = 50 mV, 100 mV and 200 mV at room temperature, T = 300K. The SET parameters are: L = 10 nm, C_G = C_S = C_D = 1aF and R_S = R_D = 1 MΩ: A) one level SET, B) Multi-level SET

Fig. 4 reproduces SET's I_D-V_D characteristics at room temperature (T = 300K) for different gate biases, V_G = 0 mV and V_G = $e/2C_G$ (Coulomb oscillation). Characteristics of metallic and semiconducting SET are shown in Fig. 4A and 4B respectively.



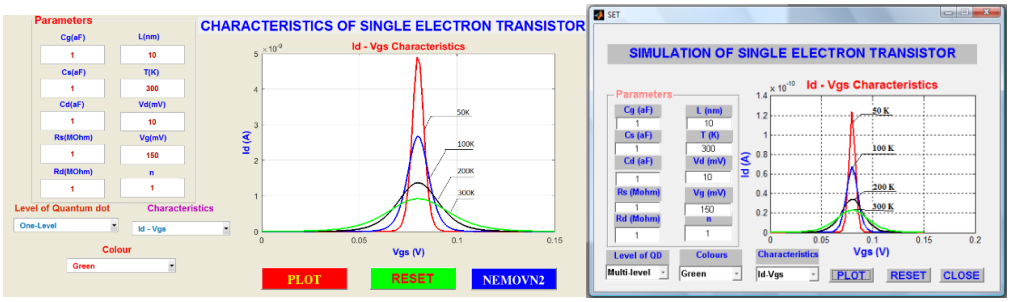
(A) (B)

Fig. 4. I_D-V_D characteristics simulated by the simulator at room temperature T = 300K for various values of V_G = 0 mV and V_G = e/2C_G. The SET parameters are: L = 10 nm, C_G = C_S = C_D = 1 aF and R_S = R_D = 1 MΩ: A) One-level SET, B) Multi-level SET

For V_G = 0 mV, V_D starts from the Coulomb blockade region and increases (or decreases) through the single-electron tunneling region. For V_G = e/2C_G (at the first Coulomb oscillation peak), I_D starts from zero and increases (or decreases) linearly. The threshold voltage of SET is V_G = e/2C_G .

Fig. 5 represents I_D-V_G characteristics with the value of V_D = 10 mV at different temperatures. One can note that the effects of temperature on Coulomb oscillations are strongly. The Coulomb oscillations of SET are clear at low temperature (at 50K). Current-voltage (I_{DS}-V_G) characteristics showing the suppression of the Coulomb oscillation by broadening current peaks increased at higher temperature (100K, 200K, and 300K). It also reveals the fact that it is no more possible to obtain the Coulomb oscillations in the device characteristics at high temperature. It should note that high temperature undermines SET's current-voltage characteristics.

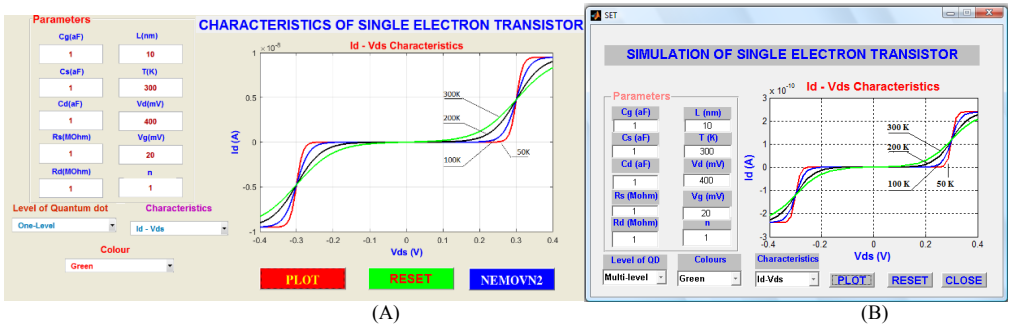
Characteristics of metallic and semiconducting SET are shown in Fig. 5A and 5B respectively.



(A) (B)

Fig. 5. Typical I_D-V_G characteristics simulated by the simulator for value of V_D = 10 mV at different temperatures: 50K, 100K, 200K, 300K. The SET device parameters are: L = 10 nm, C_G = C_S = C_D = 1aF and R_S = R_D = 1 MΩ: A) One-level, B) Multi-level

The effect of temperature (T) on the device characteristics is also demonstrated in Fig. 6, and it shows that the Coulomb blockade region becomes thinner at higher temperatures. Therefore, an accurate model for SET simulation must capture both the effect of temperature and the effect of high V_D on the device characteristics. Characteristics of metallic and semiconducting SET are shown in Fig. 6A and 6B respectively.

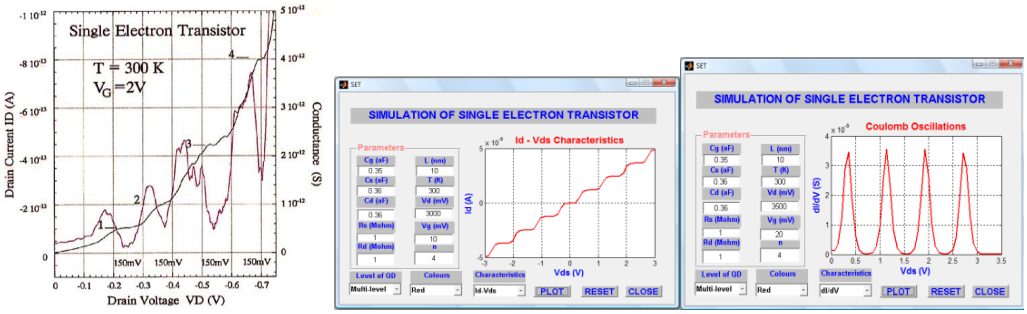


(A) (B)

Fig. 6. Typical I_{DS}-V_{DS} characteristics simulated by the simulator for value of V_G = 20 mV at different temperatures (T): 50K, 100K, 200K, and 300K. The SET device parameters are: L = 10 nm, $C_G = C_S = C_D$ = 1aF and $R_S = R_D$ = 1 MΩ: One-level SET, Multi-level SET

Accuracy of the model is evaluated by comparing simulated results with experimental ones from [8].

According to the work [8], its authors have succeeded in fabricating an SET. The SET operates at room temperature, showing a clear Coulomb staircase with a ~150 mV period at 300 K. The drain current-voltage characteristics of the SET were measured at room temperature and are shown in Fig. 7A. The gate bias was set to 2 V. In the Figure, the solid lines show the current of the SET, and the dashed line shows the conductance of the SET. Between the drain bias of 0 V and -0.75 V, four clear Coulomb staircases with a ~150 mV period are observed. The drain current versus gate bias characteristics with 150 mV drain bias at room temperature exhibit clear current oscillations with a period of ~460 mV, implying a periodic Coulomb oscillation of the current. Fig. 7B, C reproduce I_D-V_D characteristics and conductance of the same SET having length, L = 10 nm at temperature of 300 K. Fig. 7B, C show simulated results of I_D-V_D characteristics and conductance of the same SET.



A) B) C)

Fig. 7. A) Drain current versus drain voltage characteristics of the SET at 300 K [8]: V_D = 150 mV, C_t = 0.36 aF, C_G = 0.35 aF; B) I_D-V_D characteristics simulated; C) Conductance characteristics simulated by the simulator, NEMO-VN2 for value of V_G = 20 mV. The SET device parameters are: L = 10 nm, C_G = 0.35 aF, $C_S = C_D$ = 0.36 aF and $R_S = R_D$ = 1 MΩ

Four clear Coulomb staircases are shown in simulated results on I_D-V_D characteristics (Fig. 7B). Four clear conductance peaks are also shown in Fig. 7C. The results simulated according to the model coincide well with the experimental ones at least in the same shape.

CONCLUSION

Physical properties, fabrication, and the most popular simulators of SET have been introduced. A model for SET device using NEGF written in GUI of Matlab had been reported. The proposed model had been verified at one-level and multiple-level for SET's device. A set of simulations is then successfully performed for various parameters of the SET's device in one-level and multi-level modes. The model is not only able to accurately describe I_D-V_G, I_D-V_D SET's characteristics, but also affects of gate materials, size of SET, and temperature on SET's characteristics. Different SET's device characteristics (I_D-V_G, I_D-V_D, effect of temperature) have been simulated. We have found that currents in metallic SET are greater than in semiconducting SET about 100 times. The simulated results are also compared with experimental ones [8] and good agreements are validated.

Một số kết quả về tính chất vật lý của transistor đơn điện tử

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TÓM TẮT

Transistor đơn điện tử (SET) là một yếu tố cơ bản trong lĩnh vực nghiên cứu về điện tử nano và công nghệ nano hiện nay. SET cho kích thước đặc tính nano, tiêu tốn công suất thấp và tốc độ làm việc cao. SET là một linh kiện chuyển mạch thang nano mới; có thể điều khiển chuyển động của một điện tử. Mục tiêu của bài báo này là bàn về tính chất vật lý của SET và tập trung lên mô phỏng đặc trưng lượng tử cơ bản của linh kiện như hiệu ứng xuyên hầm, khóa Coulomb, chấm lượng tử, bậc thang Coulomb và dao động Coulomb. Những đặc trưng dòng-thế được nghiên cứu kỹ để minh họa. Hai loại SET kim loại và bán dẫn đã được mô phỏng.

***Từ khóa**: transistor đơn điện tử, đặc trưng dòng-thế, khóa Coulomb, bậc thang Coulomb, dao động Coulomb*

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